AMD

HyperTransport™ Technology

(previously codenamed “Lightning Data Transport” or “LDT”)

CPG Marketing

Technology Evangelism

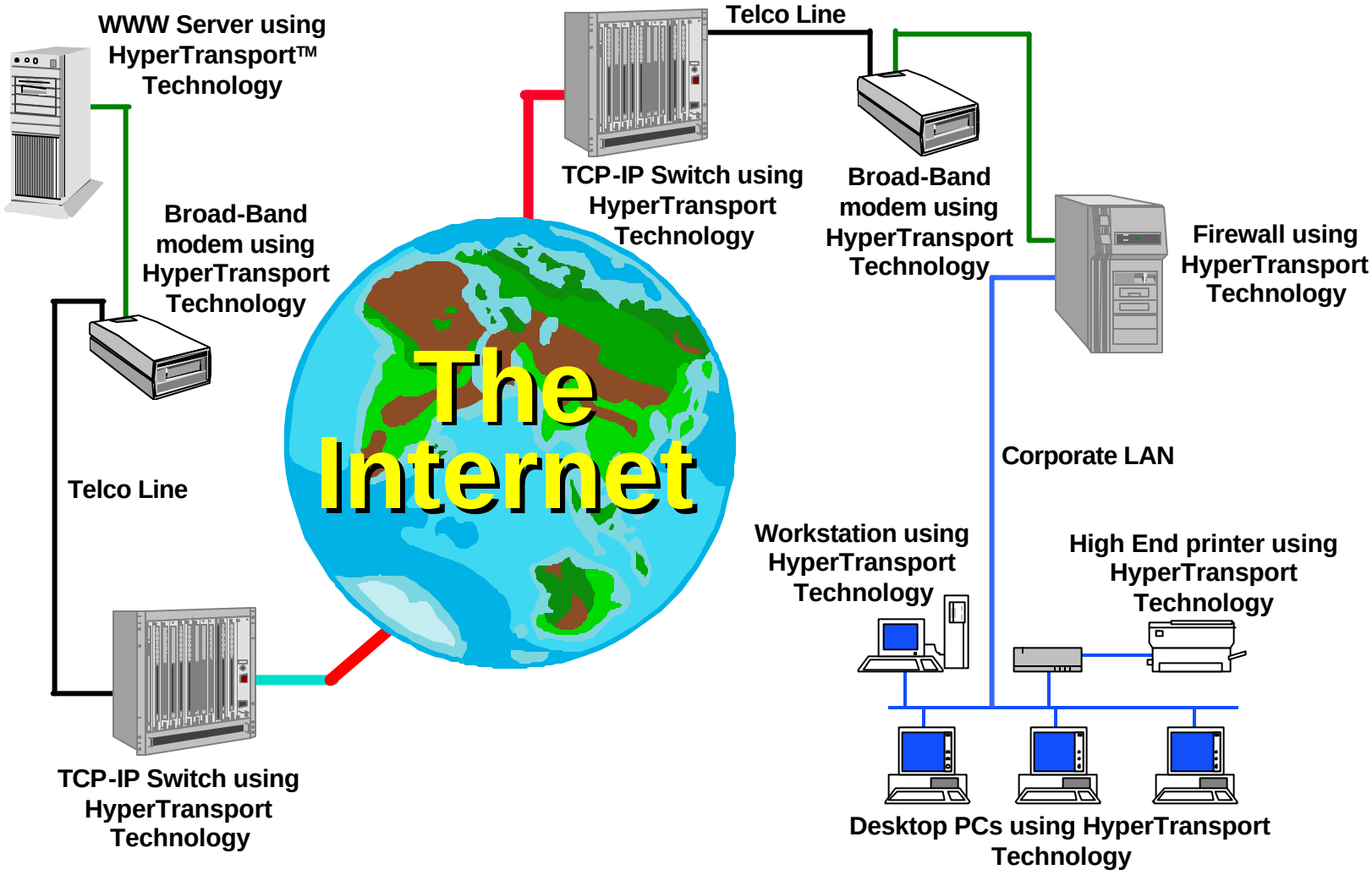
Feb 14, 2001

HyperTransport™ Technology Genealogy

AMD

- **HyperTransport™ technology was first developed for PC platforms**
  - PCI bandwidth may be insufficient for new multimedia devices being integrated into PC core logic
- **HyperTransport technology has been designed for use by servers**
  - Coherent HyperTransport technology is a high speed, low latency interconnect for NUMA architecture multiprocessing systems
- **HyperTransport technology has found a home in embedded apps**
  - RISC processors for embedded applications are being designed by HyperTransport partners
- **A wide range of devices are planned to use HyperTransport**
  - More than 50% of the HyperTransport partners are in the business to make networks run faster
  - HyperTransport is designed to be a pervasive technology in the computation, communication, networking food chain. HyperTransport is designed for Internet Acceleration!

AMD HyperTransport™ Technology is for Internet Acceleration



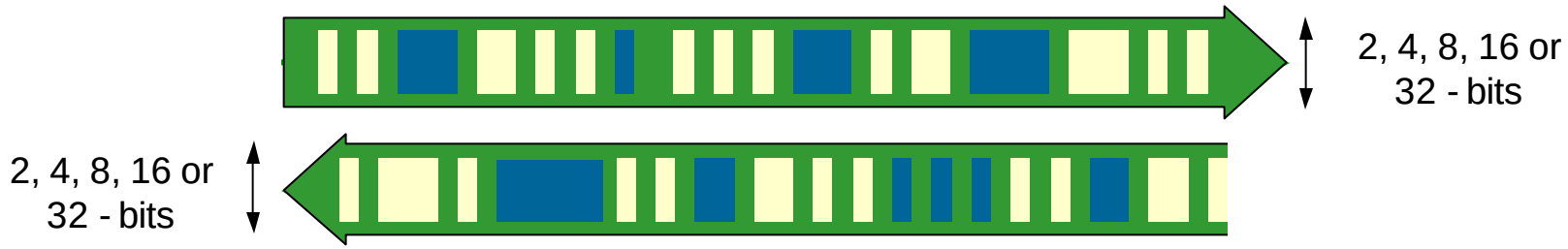
HyperTransport™ Technology

AMD

- **HyperTransport™ technology is designed to provide...**
  - a significant increase in I/O bandwidth
  - a universal link that reduces the number of buses within the system
  - support for HyperTransport tunnels that act as I/O building blocks
  - a high performance bus for embedded applications
  - a highly scalable multiprocessing systems

- **AMD is creating a next generation PC and embedded platform architecture**
  - For example: AMD PowerNow!™ Technology, HyperTransport Technology, 64-bit x86, DDR memory, and ACR initiatives
  - Plannin to offer end users outstanding performance in the industry with HyperTransport Technology

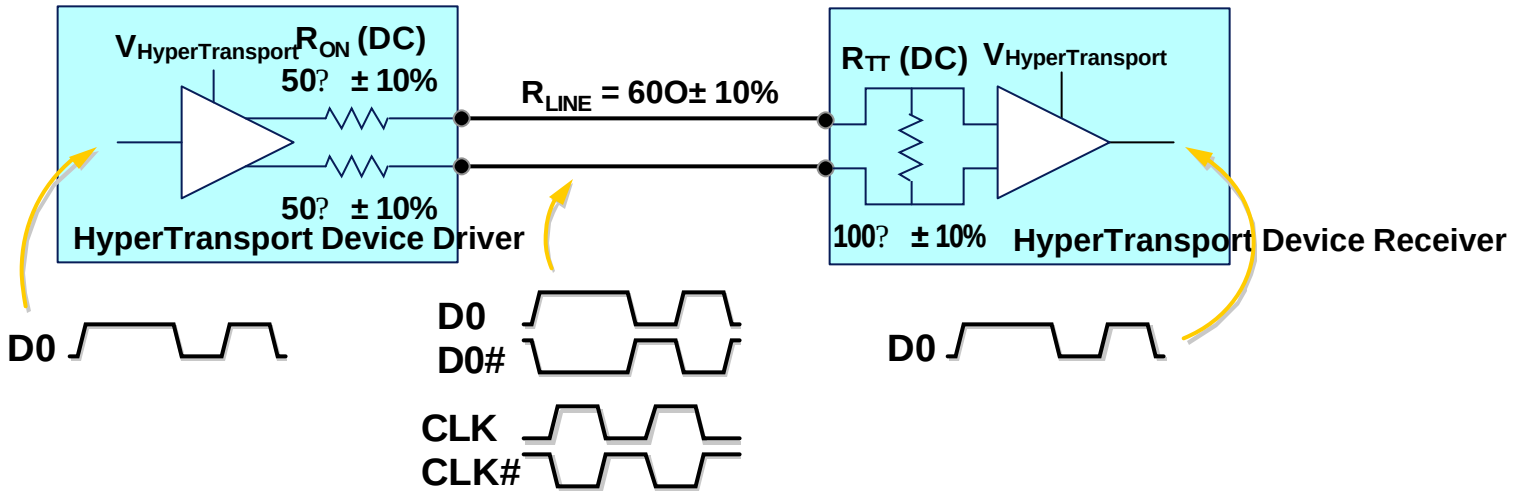
HyperTransport™ Link Basics



- **HyperTransport™ link connections have two unidirectional point-to-point links**
  - The links can be 2-, 4-, 8-, 16-, or 32-bits wide in each direction
  - HyperTransport I/O has a data rate of 800 Megabits/second per pin-pair (400 MHz clock)
    - **E.g., 8 bits each way gives 800 MB/sec each way; 1.6 GB/sec aggregate bandwidth***
    - **E.g., 4 bits each way gives 400 MB/sec each way; 800 MB/sec aggregate bandwidth***
  - For multiprocessing the CPU-to-CPU link data rate increases to 1.6 Gbits/second
    - **E.g., 16 bits each way gives 3.2 GB/sec each way; 6.4 GB/sec aggregate bandwidth***
- **Packets are multiples of 4-bytes in length**
  - On links < 32-bits, bit times concatenate to achieve the 4-byte granularity
- **Commands, addresses and data use the same bits**
  - Data packets after read responses or writes can be 4- to 64-bytes long

* The sweet spots for HyperTransport technology-based processor configurations

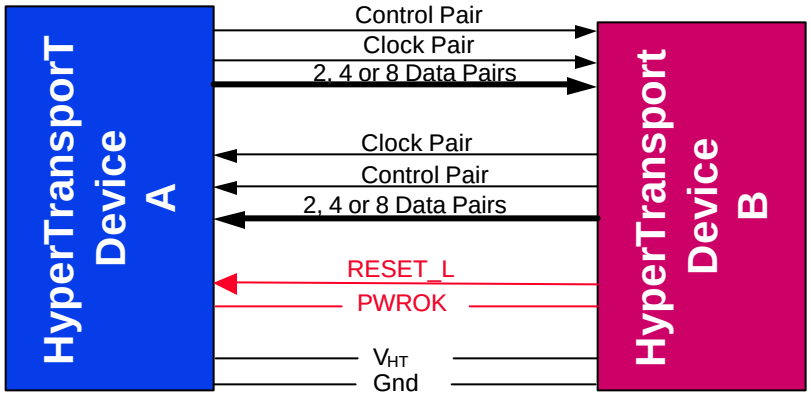
HyperTransport™ Physical Layer



- **Low voltage, differential signaling**
  - Two pins per bit - pin pairs swing in opposite directions
  - V_{HT} is 1.2 volts ± 5% resulting in a differential output of 600 $mV_{TYPICAL}$
  - Differential voltage at the receiver inputs can be as low as 200 mV
- **60 ohm differential impedance for low cost PCBs**
  - No special PCB stack-up required
  - Trace lengths up to 24 inches for 800 Mbit/sec operation

HyperTransport™ Device Pin Count

- **Additional HyperTransport signals**
  - Power OK (PWROK)
  - Reset HyperTransport Device (RESET_L)
- **55-pin HyperTransport device bus provides 12X the bandwidth of PCI-32/33 with fewer pins**
- **Signal to ground ratio is conservatively 4:1**
- **Optional link power down signals for mobile systems**
  - HyperTransportDeviceStop_L
  - DevReq_L
- **Power per pin-pair is nil when in HyperTransport Device Stop Mode**



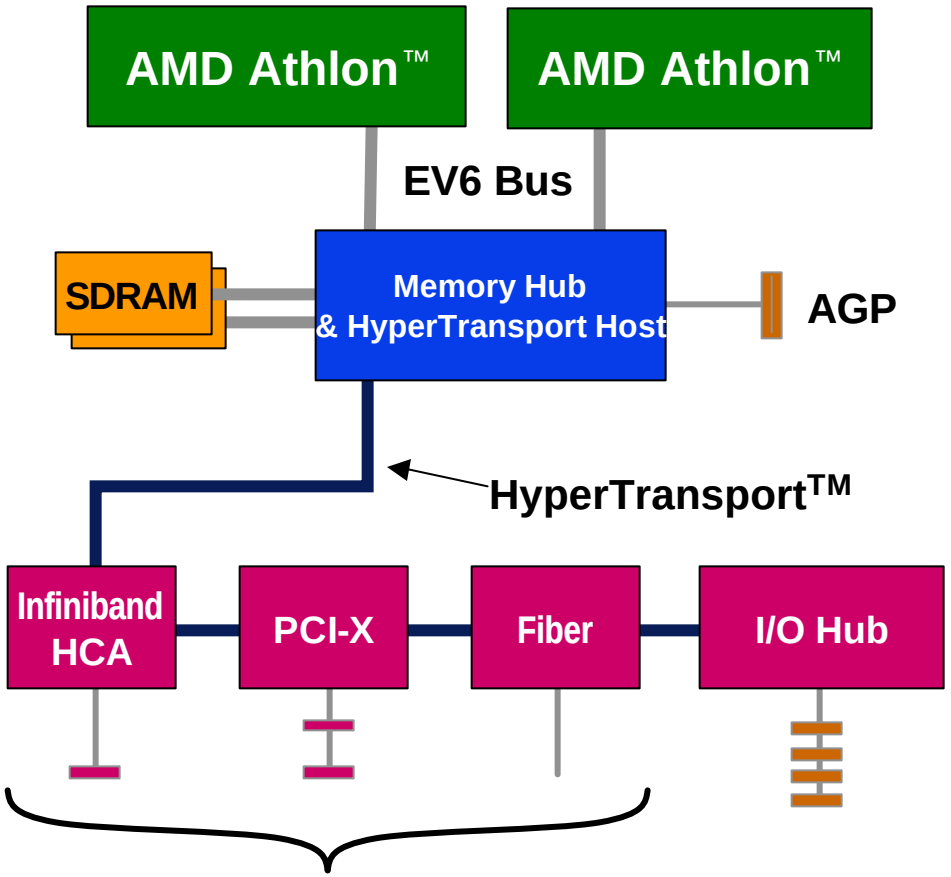
PWROK, RESET_L required for proper reset & init
V_{HT} routed between devices is required for proper common mode range

Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**

DC Power per Pin-Pair: 4 - 9 mW, 6 $mW_{Typical}$
Signal to $V_{HyperTransport}$/Gnd Ratio: 4:1

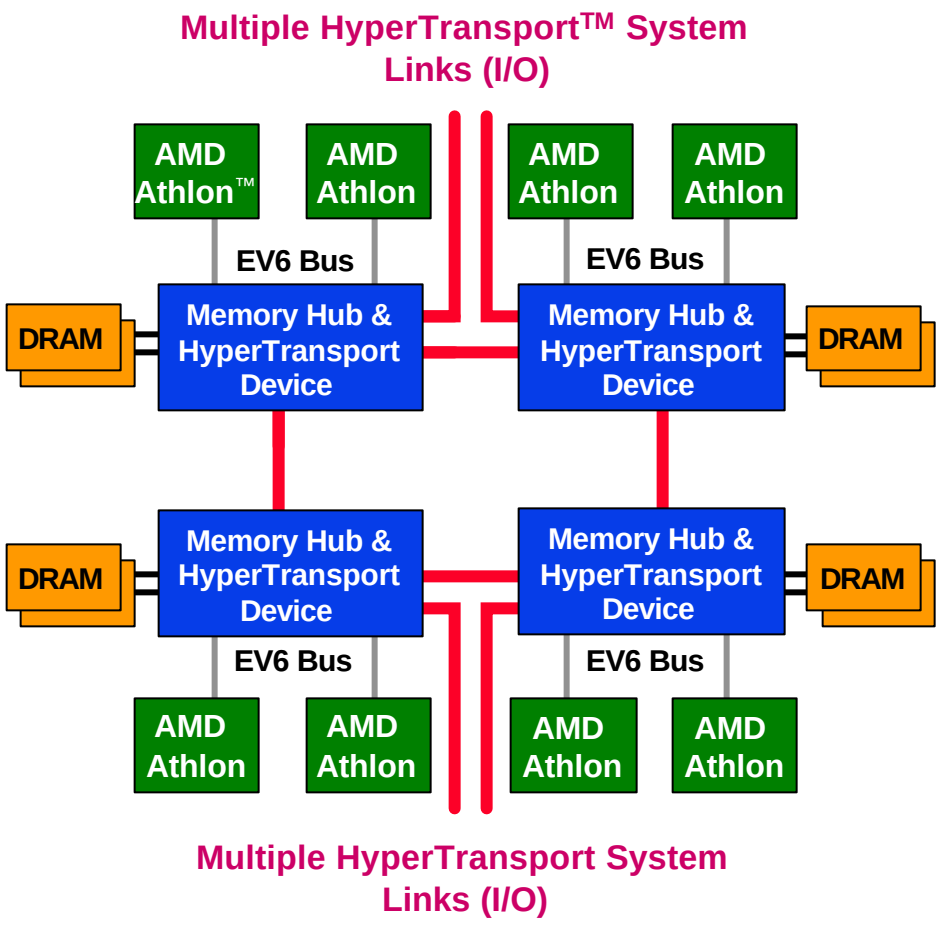
HyperTransport™ Tunnel Devices

- HyperTransport™ I/O has ample bandwidth to support daisy chained I/O devices
  - Multiple HyperTransport tunnel devices can be daisy chained on a single I/O link
  - HyperTransport bridge devices can be viewed as generic - reusable building blocks for system design
- With HyperTransport tunnels, a basic HyperTransport chipset can be designed for use in server and workstation markets



Coherent HyperTransport™ Technology-Based Multiprocessing Systems

- **Proprietary Coherent HyperTransport™ technology for interprocessor communications for SMP**
  - Coherent HyperTransport™ technology is designed to handle distant memory access in NUMA* multiprocessor systems
  - Coherent HyperTransport technology is designed to handle probes to maintain system cache coherency
- **Devices may have multiple Coherent HyperTransport ports**
  - Coherent HyperTransport technology is a proprietary superset of the HyperTransport I/O protocol, permitting Coherent HyperTransport technology based links to be used for I/O devices
- **Highly scalable SMP systems**
  - Memory capacity scales
  - Memory bandwidth scales
  - I/O capacity scales
  - I/O bandwidth scales



* **N**on-**U**niform **M**emory **A**ccess architecture - each CPU has "local" memory, but can access "distant" memory attached to other CPUs - local memory is faster than shared memory in SMP architecture, hence NUMA machines scale better in systems with large numbers of processors.

HyperTransport™ Milestones:

AMD

- **First public presentation at Microprocessor Forum 99**
- **Operational Spec version 1.0 finished in May 2000**
  - 1.01C available now (upon signing a license agreement)
- **Electrical Specs nearing completion**
- **HyperTransport presentation with technical information at WinHEC 2000**
  - Great success with about 1500 participants to our session
- **HyperTransport presentation at Platform 2000**
- **1st HyperTransport based south bridge announced by NVIDIA**
- **Sibyte (Broadcom) announced their MIPS cpu with HyperTransport**
- **Sandcraft announced their HyperTransport roadmap**
- **NDA signed by 100+ companies, list is growing**
  - about 4-5 new requests are being received each week

HyperTransport™ Milestones:

AMD

- **First licensees. Others to come soon**
  - Several companies signed, others in the pipeline
  - Numerous other companies have expressed an interest in licensing HyperTransport technology
- **NDA website established for downloading specs and technical data**
- **HyperTransport technology white paper available soon**
- **Altera first FPGA family in Q1 2001; others planned to follow**
- **Multiple HyperTransport technology based chipsets for AMD Athlon™ processors in 2001**
  - AMD chipset guys actively working to implement this technology
- **AMD has first silicon samples of a sophisticated south bridge**
  - PCI boards in house with two chips talking to each other using HyperTransport technology
- **InfiniBand solutions are in design now**
- **HyperTransport-based products are planned from AMD early 2002**
  - Partners plan to have products sooner
- **HyperTransport technology name and initial partners and promoters announced at the Platform Conference – Taipei – February 2001**
- **HyperTransport Consortium planned**
- **Further information on HyperTransport planned to be available at the WinHec 2001**

Call to Action

AMD

- **Gain access to the current HyperTransport™ technology I/O specs**
  - Sign specific HyperTransport™ technology contributor NDA
    - Specs available with login name and password
    - Access to website with specs, simulation model and names of other HyperTransport™ technology NDA-holders
- **To build and market an HyperTransport™ technology-based product**
  - Sign Licensing Contract for HyperTransport I/O Link Specification
    - Gain access to the relevent IP
- **For more information, email:**
  - gabriele.sartori@amd.com (Sunnyvale, CA)
  - chris.neuts@amd.com (Sunnyvale, CA)

Cautionary Statement

This release contains forward-looking statements, which are made pursuant to the safe harbor provisions of the U.S. Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally preceded by words such as "plans," "expects," "believes," "anticipates" or "intends." Investors are cautioned that all forward-looking statements in this release include the risks that the HyperTransport technology will not be implemented in a server or multiprocessing computer system that uses AMD processors; that the HyperTransport technology will not gain widespread industry or market acceptance; that AMD or third parties will not develop or distribute HyperTransport technology-based products in a timely manner, if at all; and that a HyperTransport consortium may not be formed by AMD. We urge investors to review in detail the risks and uncertainties in the Company's Securities and Eschange Commission filings, including the most recently filed Form-10K.